August 16, 2002 TEES
ERRATUM 1
October 27, 2003

1.3.14.1

Change the following:
"invisible when on."
To read:
"visible when on."

Note: Changes from September 8 draft are underscored with sidebar.

2. 9.2.2.2

Delete the last line that reads:

"An internal LOGIC Switch shall be provided to disconnect SP8 RTS, CTS and DCD (Pins 5, 6, 7, 18, 19 and 20) lines from C13S Connector."

9.2.3.4 RAM MEMORY

Change the first line to read:

A minimum of 8 MB of DRAM memory, organized in 32-bit words, shall be provided.

9.2.3.5 FLASH MEMORY

Replace the paragraph with the following:

" A minimum of 8 MB of FLASH memory, organized in 16- or 32- bit words, shall be provided. The MCB shall be equipped with all necessary circuitry for writing to the FLASH memory under program control. No more than 1 MB of FLASH Memory shall be used to Boot Image (List) and a minimum of 7 MB shall be available for AGENCY use. Flash memory shall have a minimum rated capacity of 100,000 read/write cycles and be industrial grade or better."

9.2.6 Data Key

Delete the last line in the second paragraph that reads:

"External capability to program the CPU Datakey shall be provided by the contractor."

Add "Type 4" and "Type 5" keys. The Key table is to read as follows:

Key Type	Model No.	Memory Size	Sector Size
1	DK1000	1Kb	1 Bite
2	LCK16000	16Kb	1 Bite
3	SFK 2Mb	2Mb	64Kbytes
4	TBD	4Mb	64Kbytes
5	TBD	8Mb	64Kbytes

9.2.7

Change the list to read as follows:

"The following shall be supplied:

1. **Operating System**
2. **Drivers and Descriptors**
3. **Application Kernel**

4. **Deliverables**
5. **Error Handler"**

9.2.7.2.3.2

Delete the following:

"error_code _os_write (path_id path, u_int32 *timer_value, u_int32 *size); Note: Prior to calling _os_write(), size must be loaded with the value 4 and timer value must be pointed to a u_int32 which contains the desired timer value as µS x 100. _os_write() shall set the desired timer value."

9.2.7.2.3.3(a)

Change:

"pb.param1 = signal; /* signal code to send (0 = cancel) */"

To read as follows:

" pb.param1 = signal; /* signal code to send (0 = do not send a signal and cancel any pending signals) */"

9.2.7.2.3.3(b)

Change:

"pb.param1 = signal; /* signal code to send (0 = cancel) */"

To read as follows:

"pb.param1 = signal; /* signal code to send (0 = do not send a signal and cancel any pending signals) */"

9.2.7.2.3.3 (c)

Replace existing paragraph with the following:

"Start timer. Start the timer if stopped. Timer will free run in a periodic mode, starting at the current timer value as its initial value and timer's maximum allowable time as its timer period (6.5535 seconds for timers 1-4 and 429496.7295 seconds for timers 12 and 34). Timer will not send a signal and any pending signals will be cancelled. Timer mode will be SS2070_Timer_Start. pb.code = SS2070_Timer_Start (0x1002); /* start timer if stopped */"

9.2.7.2.4

Change the following line:

"error_code = _os_ss_erase(path_id path, u_int32 num_sec_erase); erases sectors"

To read:

"error_code = _os_ss_erase(path_id path, u_int32 num_sec_erase); /*erases sector(s) if pointer is on a block boundary, returns E$PARAM error if not on a boundary */"

Add the following lines:

"error_code = _os_gs_pos(path_id path,u_int32 *position); /* gets current file pointer position */

error_code = _os_gs_size(path_id path, u_int32 *size); /* gets current datakey size */"

Change the sentence:

"E$EOF if upon read or write, the last byte of CPU Datakey has been processed"

To read:

"E$EOF if upon read or write, the last byte of CPU Datakey has previously been processed."

9.2.7.2.5.2 (c)

Prior to the line that reads:

"Data passed in pb->param1is defined as follows;"

Insert the following new paragraphs:

1. **If CTS is currently negated and bits 16 – 31 are not all 0:**

   Setting the SS2070_SSig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal as soon as CTS is asserted.

   Setting the SS2070_SSig parameter block bit 12 (send when CTS is negated) will cause the controller to send a one-shot signal immediately.

2. **If CTS is currently asserted and bits 16 – 31 are not all 0:**

   Setting the SS2070_SSig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal immediately.

   Setting the SS2070_SSig parameter block bit 12 (send when CTS is negated) will cause the controller to send a signal one-shot as soon as CTS is negated.

3. **If both bits 11 and 12 of the SS2070_SSig parameter block are set, and bits 16 – 31 are not all 0:**

   The controller will send a one-shot signal upon the next change of CTS state.

9.2.7.2.8

Replace existing paragraph with the following:

"The current sector of FLASH being written shall first be backed up in SRAM. The backup sector copy shall be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy. A user write operation shall restore the valid backup sector copy first. Execution of the program module, "FLRESTORE," in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay. "FLRESTORE" shall accept a delay parameter in seconds ranging from 0 to 600 seconds. The default delay factor is 30 seconds. No more that 150 KB of SRAM shall be dedicated to this purpose.

Warning: Power loss or other interruption while writing to the FLASH drive may cause FLASH drive file and/or disk corruption. It is therefore strongly recommended that the FLASH drive be used to hold controller applications only."

9.2.7.2.9

Change the paragraph:

"arp, dhcp, tftp, tftpd, ftp,ftpd, ftpdc, idbdump, idbgen, ifconfig, dhcp, inetd, ipstart,ndbmod, netstat, ping , route, routed, telnet, telnetdc, and hostname, nfsc, mount, rpcdump, nfsstat, exportfs, portmap,pppd, chat, pppauth, ndbmod, nfsd, mountd and showmount."

To read:

"arp, dhcp,___,ftp, ftpd, ftpdc, idbdump, idbgen, rpcdbgen, ifconfig, inetd, ipstart, ndbmod, netstat, ping, route, routed, telnet, telnetdc, hostname, nfsc, mount, rpcdump, nfsstat, exportfs, portmap, pppd, chat, pppauth, ____, nfsd, mountd, ___, and showmount."

Replace the wording under "Multi-user functionality" with the following:

"The boot image init module shall be configured with a "default directory name" as /f0wp. This will allow login and tsmon to provide the user with login prompt from the terminal port or from the network via a telnet session."

Change

"Network Configuration at boot up:
Factory built inetdb, inetdb2, and rpcdb shall reside in the directory /f0/CMDS/BOOTOBJS. These modules shall be configured with the network default values as defined in Section 9.2.6 (Data Key)."

To read:

"Network Configuration at boot up:

The modules inetdb, inetdb2 and rpcdb shall be generated by the make utility via the use of a makefile and the network configuration files residing the /f0/ETC directory. The generated inetdb, inetdb2 and rpcdb modules should be re-located to the /f0/CMDS/BOOTOBJS directory where they will be pick-up by the network configuration shell scripts located at /f0/SYS. The modules shall be configured with the network default values as defined in Section 9.2.6 (Data Key) via the interfaces.conf shell script."

Change the paragraph that reads:

"A Utility Program named netcfg shall be provided that reads the CPU Datakey for an IP Address, Subnet Mask and Default Gateway. If the Datakey is present and valid, netcfg shall set the IP Address, Subnet Mask and Default Gateway of the Model 2070 Controller when executed by a user at the command line or via a standard OS-9 startup file. If the Datakey is not present or invalid, netcfg shall display an error and exit without altering the network configuration. The netcfg utility shall reside in /f0/CMDS."

To read as follows:

A Utility Program named netcfg shall be provided that reads the CPU Datakey for an IP Address, Subnet Mask and Default Gateway. If the Datakey is present and valid, netcfg shall set the IP Address, Subnet Mask and Default Gateway of the Model 2070 Controller when executed by a user at the command line. The netcfg utility shall create a new inetdb, inetdb2 and rpcdb database module based on the Datakey network parameters. The new inetdb, inetdb2 and rpcdb modules should be re-located to the /f0/CMDS/BOOTOBJS directory where they will be pick-up by the network configuration shell scripts located at /f0/SYS. The netcfg shall also allow the user to read, write and display network parameters to and from the Datakey via the command line prompt.

If the Datakey is not present or invalid, netcfg shall display an error and exit without altering the network configuration. The netcfg utility shall reside in /f0/CMDS.

Remove the following paragraph (to become a separate section later):

"Standard Microware File System Configuration:
The 2070 shall follow Standard Microware File System Configuration. A /f0/CMDS, /f0/CMDS/BOOTOBJS, /f0/ETC and /f0/SYS directories should be implemented. The/f0/CMDS directory shall contain the network modules mentioned above as well any other modules not part of the OS-9 boot image. Execute permission shall be included in the attributes of files in the /f0/CMDS directory. Sysgo should set its execution directory to /f0wp/CMDS prior to spawning opexec or other processes. The /f0/CMDS/BOOTOBJS shall contain the modules as identified above and other

customizable descriptors and modules. The /f0/SYS should contain a "password" file. The password file should follow Microware's password file format for the addition and configuration of multiuserc functionality and password protection."

Change the line that reads:
" hosts, hosts.equiv, networks, protocols, services, inetd.conf, resolv.conf, hosts.conf, rpc, interfaces.conf, routes.conf."

To read:
"hosts, hosts.equiv, networks, protocols, services, inetd.conf, resolv.conf, hosts.conf, rpc, interfaces.conf, routes.conf. makefile, nfs.map, nfsd.map"

Insert the following new paragraphs:

9.2.7.2.10 STANDARD MICROWARE FILE SYSTEM CONFIGURATION

9.2.7.2.10.1

The 2070 shall follow Standard Microware File System Configuration. A /f0/CMDS, /f0/CMDS/BOOTOBJS, /f0/ETC and /f0/SYS directories shall be implemented. Execute permission shall be included in the attributes of files in the /f0/CMDS directory. Sysgo should set its execution directory to /f0wp/CMDS prior to spawning opexec or other processes. The /f0/CMDS/BOOTOBJS shall contain the modules as identified above and other customizable descriptors and modules. The /f0/SYS shall also contain the following four standard OS-9 network configuration shell script files: startspf, startnfs, loadspf and loadnfs.

9.2.7.2.10.2

The /f0/SYS shall contain a "password" file. The password file should follow Microware's password file format for the addition and configuration of multiuser functionality and password protection. A user name "super" with password as "user" shall be defined in the password file.

9.2.7.2.10.3
The utilities tar, make, fixmod and mshell shall be included in the /f0/CMDS directory.

9.2.7.3.3

Replace existing paragraph to read:

Initialization
The boot image init module shall be configured with a "default directory name" as /f0wp. This action will direct the OS9 kernel to set the current directory to /f0wp and set the execution directory to /f0wp prior to Sysgo starting.

After initialization (boot up from SYSRESET) :

1. **Sysgo shall set the execution directory to /f0wp/CMDS**
2. **Sysgo shall check if the backspace key (0x08) is being transmitted from aterminal device attached to /sp4 (c50s):**
   a. **If received, the Sysgo shall fork a shell on /sp4 using the current directory.**
   b. **Sysgo will remain an active process and will monitor the shell for termination. If the shell does terminate, Sysgo will fork another shell on /sp4. Unless Sysgo dies, a shell will always be provided on /sp4.**
3. **If the backspace key has not been received:**
   a. **Sysgo shall fork the module named /f0wp/OPEXEC if present at /f0wp.**

b. If forking OPEXEC does not return any errors, Sysgo will then exit without forking a shell.

c. If forking OPEXEC does return an error, Sysgo will fork a terminal shell on /sp4 using the current directory

4. If the backspace key has not been received and there is no OPEXEC file present:

a. Sysgo shall fork a shell that executes a standard OS-9 startup file named /f0wp/startup if present at /f0wp.

b. Sysgo will remain an active process and will monitor the shell for termination. If the shell does terminate, Sysgo will fork another shell on /sp4. Unless Sysgo dies, a shell will always be provided on /sp4.

5. If the backspace key has not been received and there is no OPEXEC and no startup file present:

a. Sysgo shall fork a shell on /sp4 using the current directory.

b. Sysgo will remain an active process and will monitor the shell for termination. If the shell does terminate, Sysgo will fork another shell on /sp4. Unless Sysgo dies, a shell will always be provided on /sp4.

9.2.7.4.1

Replace existing paragraph to read:

"A manufacturer may include an error handling routine to save troubleshooting data regarding initialization, power-up test abnormalities and other error conditions. If used, the error report shall be stored in the file /r0/ErrorReport and shall not exceed 11kb in size."

9.2.7.4.2

Delete this Section

9.2.7.4.3

Delete this Section

9.2.7.7.1

Replace existing paragraph to read as follows:

2 copies of the following items will be provided to the purchasing AGENCY on a CD disk readable by a PC compatible computer.

1. Specific hardware memory addresses, including FLASH, SRAM, and DRAM starting addresses, shall be specified and provided. Written documentation of addresses shall be in PDF form and will have the file name of "Memory Map.pdf"

2. Copies of the vendor kernel, platform drivers and OS-9 utility executable modules.

3. Copy of all provided written manuals in PDF form.

4. RE-FLASH Utility and the procedures for its use in PDF form. The PDF documentation of the procedures shall have the file name of "Reflash Utility Procedures.pdf".

9.2.7.7.2

Replace existing paragraph to read:

"Fully commented source code of Contractor developed drivers and utilities shall be provided."

9.2.7.7.3

Replace existing paragraph to read:

"OS-9 compliant header files shall be provided with all driver modules."

9.2.7.7.4

Delete this paragraph

9.2.7.7.5

Delete this paragraph

9.2.7.7.6

Delete this paragraph

9.3.5.2

Change:

"every 100 ms for 3.5 seconds"

To read:

"every 100 ms for 10 seconds".

Page 9-7-1

Move the PS1 and PS2 connectors on the picture to the right side of the power supply

Change note 4 to read:

"The length of the Front Panel Harness shall be no less than 125mm."

Page 9-7-2

Add a new note:

"5. Power supply will be marked with 2070-4A or 2070-4B".

Page 9-7-7

Changes the "A2 to A5 Connector Pin Out" table to read as follows:

A2 TO A5 CONNECTOR PIN OUT			
LOGICAL PORT	**68360 PORT**	**RATE KBITS**	**PROTOCOL**
SP1	**SEE NOTE 4**	**(1)**	**ASYNC**
SP1S	**SEE NOTE 4**	**(2)**	**SYNC, HDLC, SDLC**
SP2	**SCC2**	**(1)**	**ASYNC**
SP2S	**SCC2**	**(2)**	**SYNC, HDLC, SDLC**
SP3	**SCC4**	**(1)**	**ASYNC**
SP3S	**SCC4**	**153.6, 614.4***	**SYNC, HDLC, SDLC**
SP4	**SMC2**	**(1) , 9.6***	**ASYNC**
SP5	**SCC3**	**(1)**	**SYNC, HDLC, SDLC**
SP5S	**SCC3**	**153.6, 614.4***	**ASYNC**
SP6	**SMC1**	**(1), 38.4***	**SYNC, HDLC, SDLC**
SP8**	**SEE NOTE 4**	**9.6***	**ASYNC**
SP8s**	**SEE NOTE 4**	**153.6, 614.4**	**SYNC**

Delete from C13 Pin Assignment table:

"" were applicable.**

Delete under Note 3:

" Disconnected by internal switch"**

Add to Note 4:

SP8 of the 2070-1B is assigned to the Dual SCC

Add a new Note:

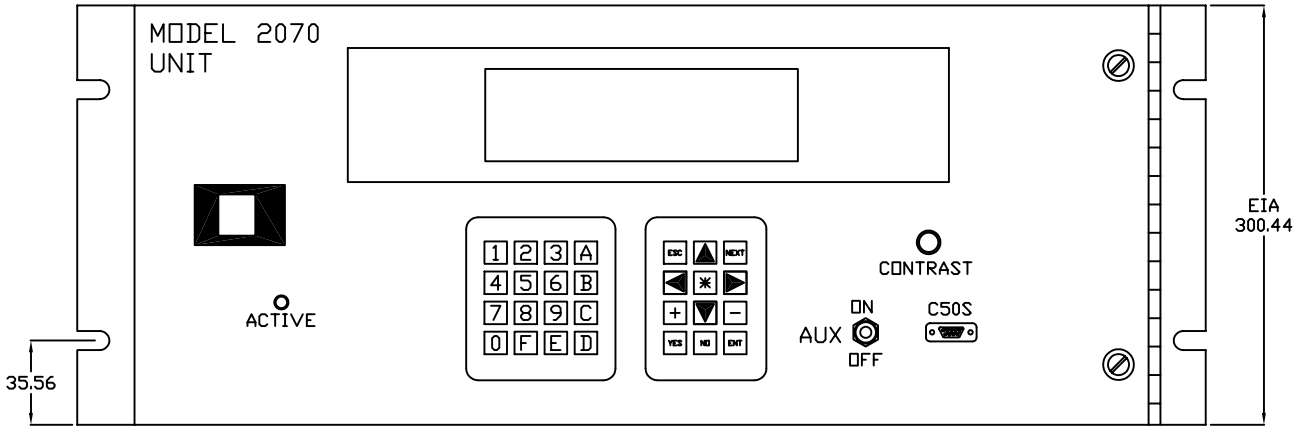
"6. ** 2070-1B CPU only"

Page 9-7-13

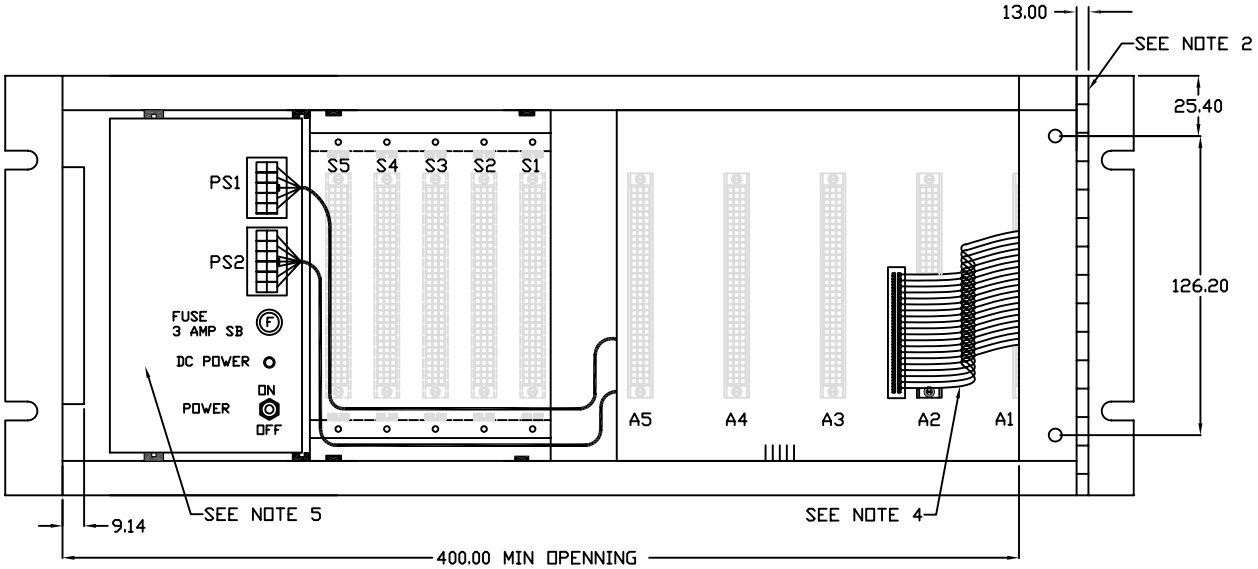
Move the PS1 and PS2 connectors on the picture to the right side of the power supply

Add a new note:

"8. Power supply will be marked with 2070-4A or 2070-4B".



FRONT PANEL INSTALLED



FRONT PANEL REMOVED

NOTES (THIS DETAIL)

1. The unit shall be capable of mounting to a Standard EIA-310B Rack using 4U open end mounting slots.

2. Continuous stainless steel hinge (4mm maximum hinge barrel) that attaches to the Front Panel by two TSD #1 Thumbscrew devices.

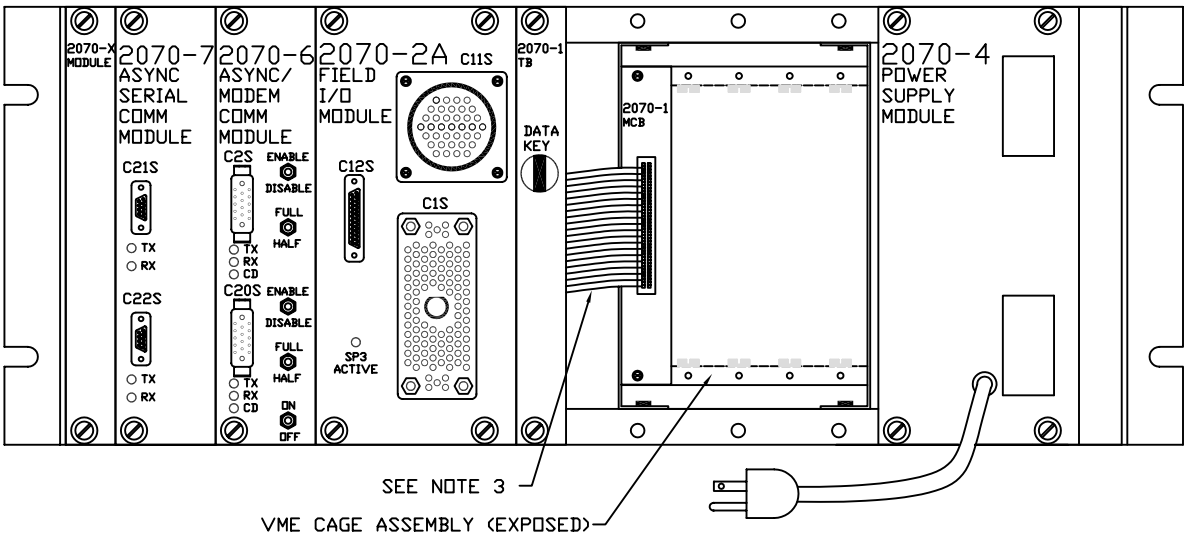
3. Actual location of ACTIVE light and contrast control shall be limited to ACTIVE light on the left side of the panel and the contrast control on the right side. They shall be located greater than 25.4 mm from other devices, connector or latch.

4. The length of the Front Panel Harness shall be no less than 125 mm.

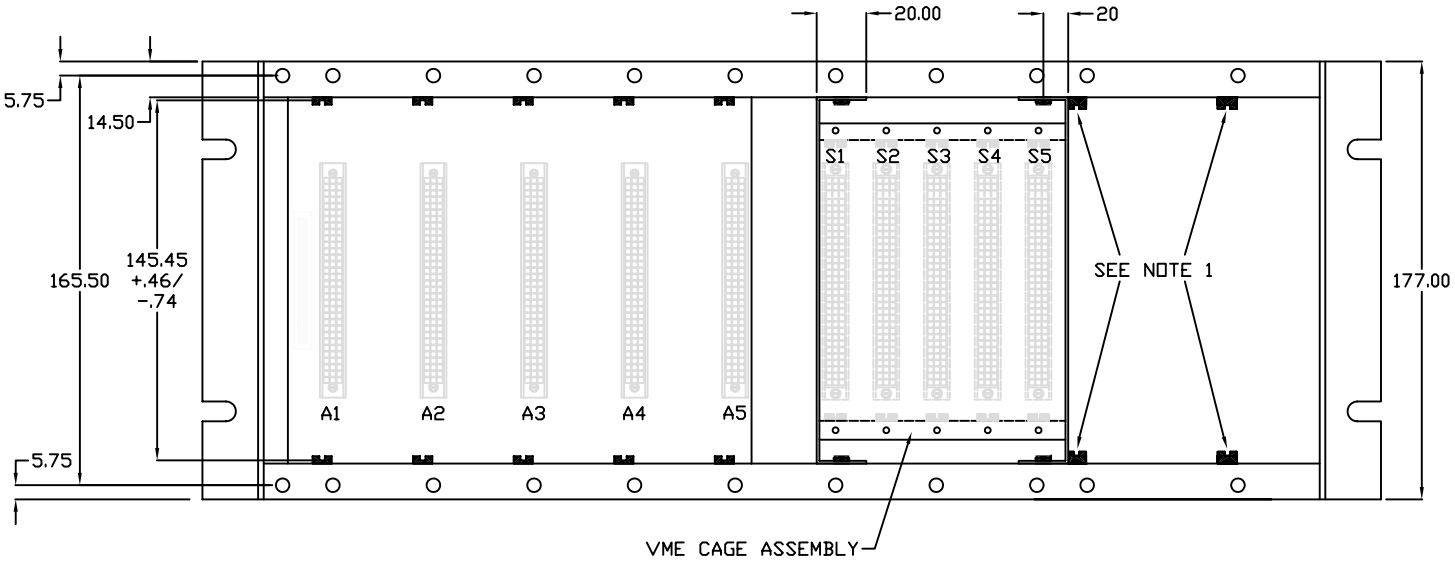
5. A LED indicator for each DC voltage shall be provided.

6. With the hinge installed, the distance between the TSD hole center & the CHASSIS Right Side (inside plane) shall be 14.00 mm

	TITLE: MODEL 2070 CHASSIS FRONT VIEW	
	NO SCALE	
	OCTOBER 27, 2003	9-7-1



REAR VIEW, LOADED



REAR VIEW, UNLOADED

NOTES (THIS DETAIL)

1. Four permanently attached 203.2 mm long Card Guides SAE 1800F (OR EQUAL) beginning 13 mm from the backplane mounting surface.

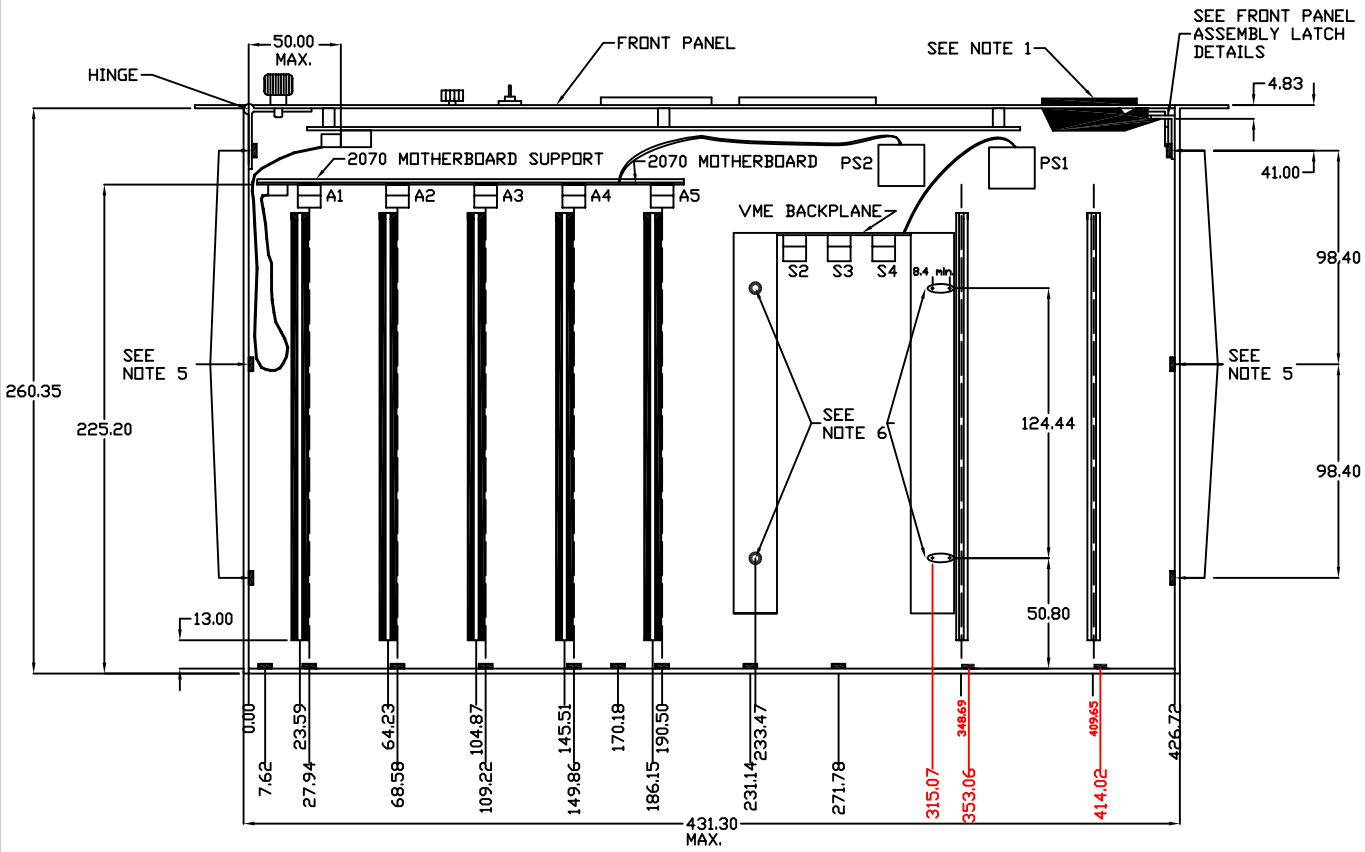
2. TB - TRANSITION BOARD
   MCB - MAIN CONTROLLER BOARD

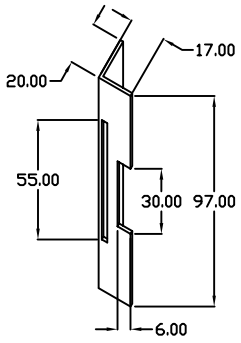
3. Maximum length of harness shall be 101.60 mm, and shall not protrude beyond the back of the 2070 unit.

4. The VME Cage Assembly Openning shall be delivered covered by a blank panel. Matching M3 PEM fasteners shall be provided on the back plane surface for panel mounting.

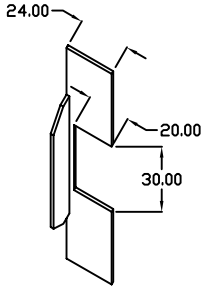
5. Power Supply will be marked with 2070-4A or 2070-4B

TITLE: MODEL 2070 CHASSIS REAR VIEW	
NO SCALE OCTOBER 27, 2003	9-7-2

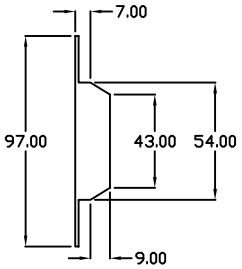




CHASSIS BRACKET



FRONT PANEL BRACKET



SIDE VIEW

FRONT PANEL ASSEMBLY LATCH DETAILS

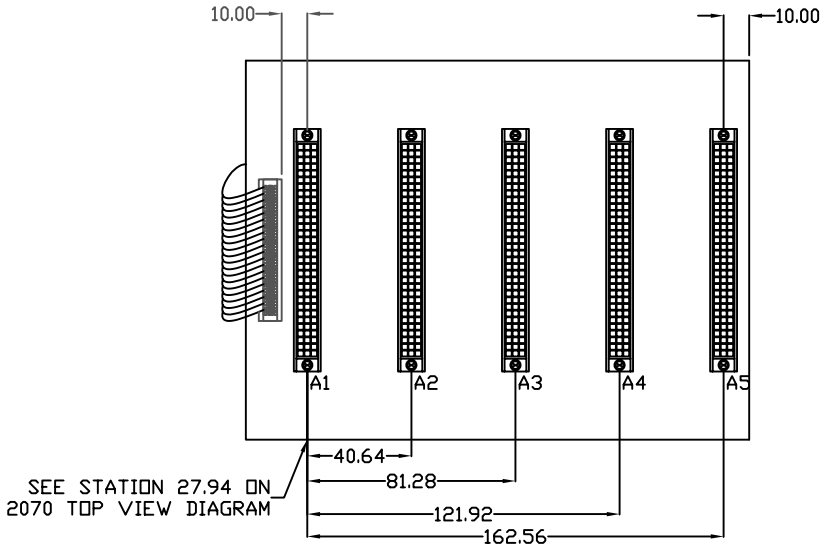
NOTES (THIS DETAIL)

1. Front Panel Assembly Latch mating with and rigidly held in place by Chassis Guide Latch/member shall be provided. The member shall vertically support the Front Panel Assembly in two other points besides the Latch.
2. Nylon card guides, SAE 1800F (OR EQUAL), shall be provided (top and bottom) for Mother Slot/Connectors A1 to A5. The Guides shall begin 13 mm from the Backplane surface.
3. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes located on Backplane Surface.
4. All harnesses shall have a minimum slack of 25 mm when connected.
5. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the TSD #3 Thumbscrew Devices on the Model 2070-8 Module. Fastener centers shall be 6.35 mm above unit baseline.
6. Eight 6-32 Phillips head counter-sunk screws, 4 top and 4 bottom, shall be used to mount the cage assembly to the 2070 Chassis.
7. The 2070 chassis top & bottom sections shall be constructed with a continuous 15.77 mm folded lip along the front perpendicular to the 2070 top and bottom sections. The top and bottom sections of the 2070 chassis shall be recessed 18 mm as measured from the front surface of the front panel.

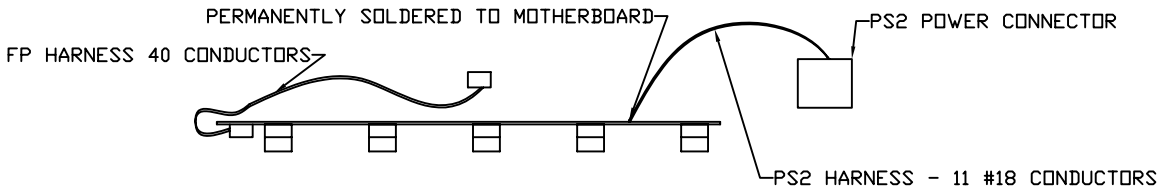
TITLE:

MODEL 2070 CHASSIS TOP VIEW

	NO SCALE	
	OCTOBER 27, 2003	9-7-3



FRONT VIEW



TOP VIEW

FP HARNESS PIN/WIRING ASSIGNMENT			
PIN	CONNECTOR ROW A	PIN	CONNECTOR ROW B
1	SP4-TXD+	2	SP4-TXD-
3	SP4-RXD+	4	SP4-RXD-
5	SP6-TXD+	6	SP6-TXD-
7	SP6-RXD+	8	SP6-RXD-
9	NA	10	NA
11	NA	12	NA
13	NA	14	NA
15	NA	16	NA
17	NA	18	NA
19	NA	20	NA
21	DC GROUND #1	22	DC GROUND #1
23	+12 VDC SERIAL	24	-12 VDC SERIAL
25	DC GROUND #1	26	DC GROUND #1
27	CPU LED	28	DC GROUND #1
29	CPURESET	30	DC GROUND #1
31	DC GROUND #1	32	C50 ENABLE
33	DC GROUND #1	34	+5 VDC
35	+5 VDC	36	+5 VDC
37	+5 VDC	38	+5 VDC
39	NA	40	NA

PS2 HARNESS PIN/WIRING ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC - ISOLATED
7	DC GROUND #2 (+12 VDC ONLY)
8	POWER DOWN
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

NOTES (THIS DETAIL)

1. The Motherboard shall be a 3.175 mm minimum thickness pcb mechanically mounted in a vertical position.

2. A1 to A5 receptacle connectors shall be 96 socket contact DIN 41612 connectors (ROBINSON NUGENT #DIN 96RSC or ELCO Series 8477 Three Row Inverted Socket OR EQUAL).

3. The FP Harness may be located on either side of the motherboard. The FP Harness shall either be directly soldered to the motherboard or a header used.

TITLE:

MODEL 2070 CHASSIS MOTHERBOARD

NO SCALE

OCTOBER 27, 2003

A1 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP3TXD+	SP6TXD+	SP5TXD+
2	SP3TXD-	SP6TXD-	SP5TXD-
3	SP3RXD+	SP6RXD+	SP5TXC+
4	SP3RXD-	SP6RXD-	SP5TXC-
5	SP3RTS+	SP3TXC□+	SP5RXD+
6	SP3RTS-	SP3TXC□-	SP5RXD-
7	SP3CTS+	SP3TXCI+	SP5RXC+
8	SP3CTS-	SP3TXCI-	SP5RXC-
9	SP3DCD+	SP3RXC+	SP3TXD+
10	SP3DCD-	SP3RXC-	SP3TXD-
11	SP4TXD+	SP4TXD+	SP3RXD+
12	SP4TXD-	SP4TXD-	SP3RXD-
13	SP4RXD+	SP4RXD+	SP3RTS+
14	SP4RXD-	SP4RXD-	SP3RTS-
15	NA	NA	SP3CTS+
16	NA	NA	SP3CTS-
17	NA	NA	SP3DCD+
18	NA	NA	SP3DCD-
19	NA	NA	SP3TXC□+
20	NA	NA	SP3TXC□-
21	DCG #1	C50 ENABLE	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

A2 TO A5 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP1TXD+	SP6TXD+	SP5TXD+
2	SP1TXD-	SP6TXD-	SP5TXD-
3	SP1RXD+	SP6RXD+	SP5TXC+
4	SP1RXD-	SP6RXD-	SP5TXC-
5	SP1RTS+	SP1TXC0+	SP5RXD+
6	SP1RTS-	SP1TXC0-	SP5RXD-
7	SP1CTS+	SP1TXCI+	SP5RXC+
8	SP1CTS-	SP1TXCI-	SP5RXC-
9	SP1DCD+	SP1RXC+	SP3TXD+
10	SP1DCD-	SP1RXC-	SP3TXD-
11	SP2TXD+	SP4TXD+	SP3RXD+
12	SP2TXD-	SP4TXD-	SP3RXD-
13	SP2RXD+	SP4RXD+	SP3RTS+
14	SP2RXD-	SP4RXD-	SP3RTS-
15	SP2RTS+	SP2TXC□+	SP3CTS+
16	SP2RTS-	SP2TXC□-	SP3CTS-
17	SP2CTS+	SP2TXCI+	SP3DCD+
18	SP2CTS-	SP2TXCI-	SP3DCD-
19	SP2DCD+	SP2RXC+	SP3TXC□+
20	SP2DCD-	SP2RXC-	SP3TXC□-
21	DCG #1	NA	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

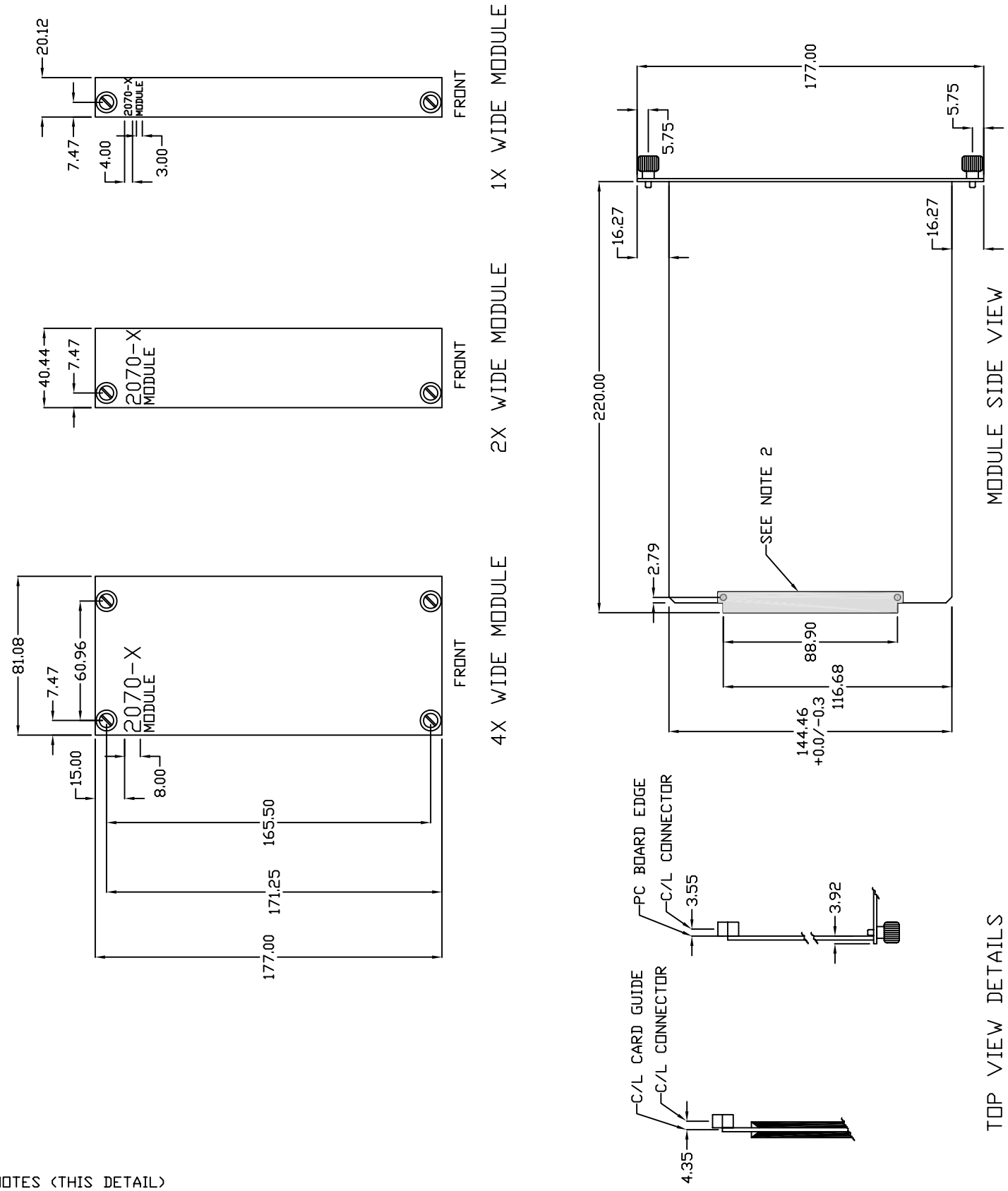
NOTES (THIS DETAIL)

1. Functions are referenced to the CPU.
2. DC GND #1 for +5VDC and +12VDC Serial. DC GND #2 for +12VDC ISO.
3. A1 Connector is the furthest A Connector to the left when viewed from the unit back. All A Connectors are pin assigned the same.
4. Connector A2 to A4, pins B21 and B22 shall read "NA".
   Connector A2, pins B23 shall read "A2 Installed".
   Connector A3, pins B23 shall read "A3 Installed".
   Connector A4, pins B23 shall read "NA".
   Connector A5, pins B21 shall read "A2 Installed".
   Connector A5, pins B22 shall read "DCG #1".
   Connector A5, pins B23 shall read "A3 Installed".
5. Pin A24 (DCG #1) is reserved for network protection only, ie., "Ethernet Shield".
6. Connector A2 installed, enables SP1 and SP2.
7. Connector A3 install, enbales SP5.
8. SP3 and SP6 are always enabled.
9. C50 enabled, disconnects SP4 on connector A1.

TITLE:

Motherboard A Connector Pin Assignment

NO SCALE	
OCTOBER 27, 2003	9-7-5



NOTES (THIS DETAIL)

1. All Thumbscrew devices on modules described in this drawing shall be TD#3 OR EQUAL.

2. 96 pin DIN connector ELCO # 00 8272 96 000 013 OR EQUAL.

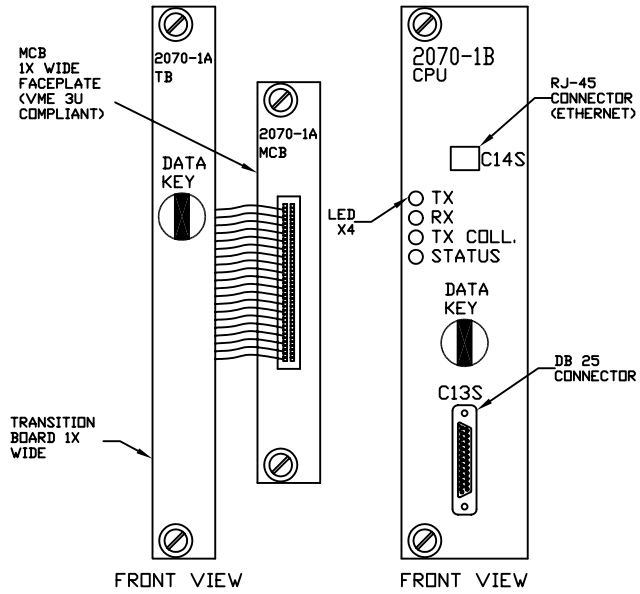
TITLE: MODEL 2070 SYSTEM PCB MODULES, GENERAL

	NO SCALE	
	OCTOBER 27, 2003	9-7-6

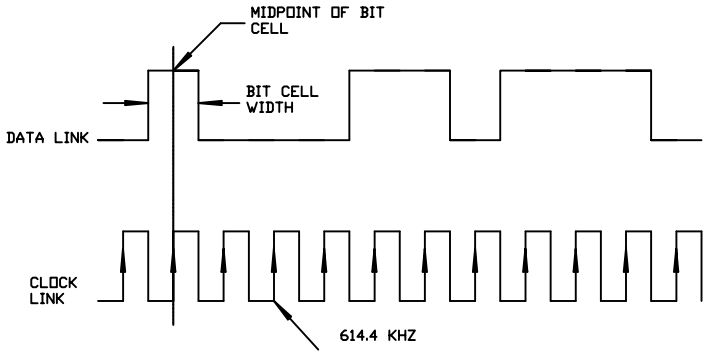
SERIAL PORT REQUIREMENTS

A2 TO A5 CONNECTOR PIN OUT			
LOGICAL PORT	68360 PORT	RATE KBITS	PROTOCOL
SP1	SEE NOTE 4	(1)	ASYNC
SP1S	SEE NOTE 4	(2)	SYNC, HDLC, SDLC
SP2	SCC2	(1)	ASYNC
SP2S	SCC2	(2)	SYNC, HDLC, SDLC
SP3	SCC4	(1)	ASYNC
SP3S	SCC4	153.6, 614.4*	SYNC, HDLC, SDLC
SP4	SMC2	(1), 9.6*	ASYNC
SP5	SCC3	(1)	ASYNC
SP5S	SCC3	153.6, 614.4*	SYNC, HDLC, SDLC
SP6	SMC1	(1), 38.4*	ASYNC
SP8**	SEE NOTE 4	9.6**	ASYNC
SP8**	SEE NOTE 4	153.6, 614.4	SYNC, HDLC, SDLC

SDLC FRAME LAYOUT					
OPENNING FLAG	ADDR	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	1000 0011	VARIABLE LENGTH	16 BITS	0111 1110



CPU FACE PANELS



SDLC TIMING

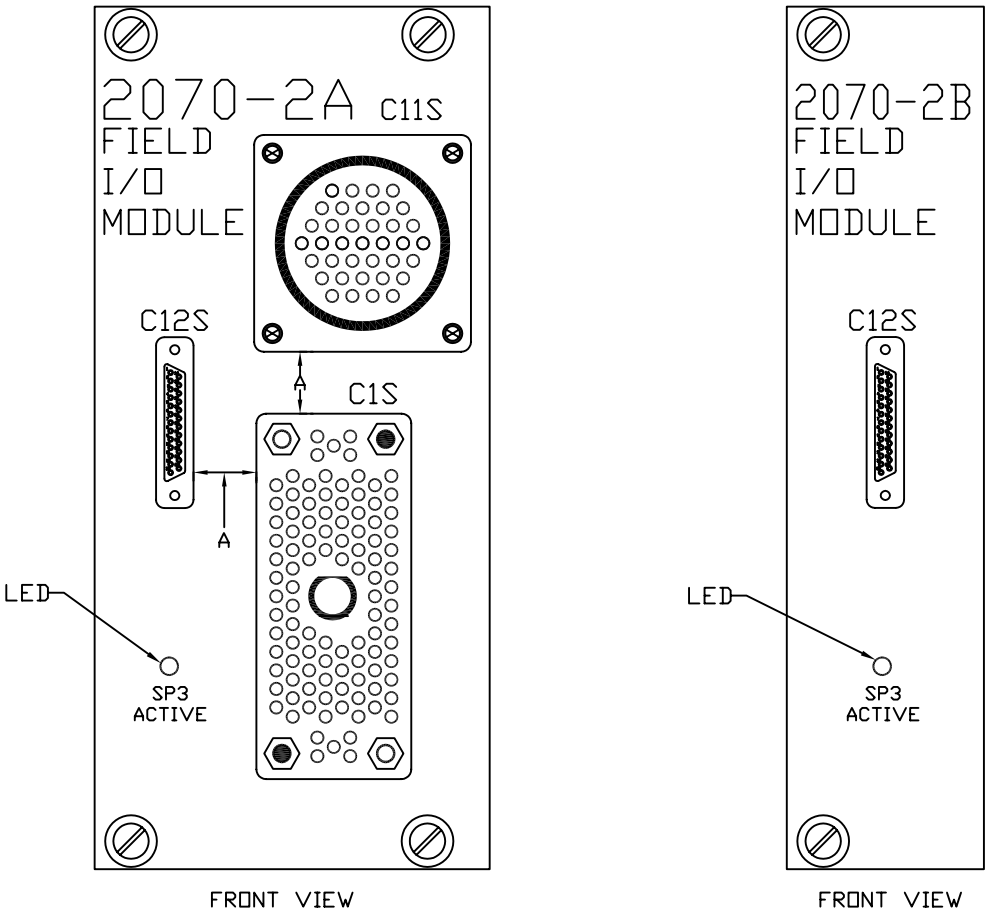
C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS +	18	SP8 RTS -
6	SP8 CTS +	19	SP8 CTS -
7	SP8 DCD +	20	SP8 DCD -
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

C14S PIN ASSIGNMENT (ETHERNET)			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES (THIS DETAIL)

1. (1) BPS Rates 1.2* 2.4, 4.8, 9.6, 19.2, 38.4
2. (2) BPS Rates 19.2*, 38.4, 57.6, 76.8, 153.6
3. * Default BPS Rate for indicated Port.
4. SP1 OF THE 2070-1A is 68360 SCC1. SP1 OF THE 2070-1B is Dual SCC1 with 68360 SCC1 assigned to ETHERNET. SP8 of the 2070-1B is assigned to the Dual SCC.
5. A Post Header (ROBINSON NUGENT IDA-XX OR EQUAL) Connector with strain relief shall be provided on the MCB Front Plate and the Transition Board for mating with the interface harness. The harness shall be shielded and straight through wired.
6. ** 2070-1B only

TITLE: MODEL 2070-1 CPU MODULES AND SERIAL PORT/SDLC PROTOCOL	
NO SCALE	9-7-7
OCTOBER 27, 2003	



FIELD I/O FACE PANELS

NOTES (THIS DETAIL)

1. 2070-2A Faceplate shall be 4X wide. 2070-2B Faceplate shall be 2X wide. (SEE SYSTEM PCB MODULE, GENERAL DETAILS.)

2. Dark Circles in the C1S Connector denote guide pin locations and open circles denote guide socket locations.

3. Dimension "A" shall be a minimum of 12.7 mm.

4. C1S - M104 Type
   C11S - 37-Pin Circular Plastic Type
   C12S - 25-Pin DB Socket Type

5. C12S PIN 12 (+5VDC) IS DERIVED from Isolated +12 VDC Power Supply

C12S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX5 DATA +	14	TX5 DATA -
2	RX5 DATA +	15	RX5 DATA -
3	TX5 CLOCK +	16	TX5 CLOCK -
4	RX5 CLOCK +	17	RX5 CLOCK -
5	TX3 DATA +	18	TX3 DATA -
6	RX3 DATA +	19	RX3 DATA -
7	TX3 CLOCK +	20	TX3 CLOCK -
8	RX3 CLOCK +	21	RX3 CLOCK -
9	LINE SYNC +	22	LINE SYNC -
10	NRESET +	23	NRESET -
11	POWER DOWN +	24	POWER DOWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

TITLE:

MODEL 2070-2
FIELD I/O MODULES

	NO SCALE	
	OCTOBER 27, 2003	9-7-8

C1S PIN ASSIGNMENT

PIN	FUNCTION	
	NAME	PORT
1	DC GROUND	
2	□0	□1-1
3	□1	□1-2
4	□2	□1-3
5	□3	□1-4
6	□4	□1-5
7	□5	□1-6
8	□6	□1-7
9	□7	□1-8
10	□8	□2-1
11	□9	□2-2
12	□10	□2-3
13	□11	□2-4
14	DC GROUND	
15	□12	□2-5
16	□13	□2-6
17	□14	□2-7
18	□15	□2-8
19	□16	□3-1
20	□17	□3-2
21	□18	□3-3
22	□19	□3-4
23	□20	□3-5
24	□21	□3-6
25	□22	□3-7
26	□23	□3-8

PIN	FUNCTION	
	NAME	PORT
27	□24	□4-1
28	□25	□4-2
29	□26	□4-3
30	□27	□4-4
31	□28	□4-5
32	□29	□4-6
33	□30	□4-7
34	□31	□4-8
35	□32	□5-1
36	□33	□5-2
37	□34	□5-3
38	□35	□5-4
39	I0	I1-1
40	I1	I1-2
41	I2	I1-3
42	I3	I1-4
43	I4	I1-5
44	I5	I1-6
45	I6	I1-7
46	I7	I1-8
47	I8	I2-1
48	I9	I2-2
49	I10	I2-3
50	I11	I2-4
51	I12	I2-5
52	I13	I2-6

PIN	FUNCTION	
	NAME	PORT
53	I14	I2-7
54	I15	I2-8
55	I16	I3-1
56	I17	I3-2
57	I18	I3-3
58	I19	I3-4
59	I20	I3-5
60	I21	I3-6
61	I22	I3-7
62	I23	I3-8
63	I28	I4-5
64	I29	I4-6
65	I30	I4-7
66	I31	I4-8
67	I32	I5-1
68	I33	I5-2
69	I34	I5-3
70	I35	I5-4
71	I36	I5-5
72	I37	I5-6
73	I38	I5-7
74	I39	I5-8
75	I40	I6-1
76	I41	I6-2
77	I42	I6-3
78	I43	I6-4

PIN	FUNCTION	
	NAME	PORT
79	I44	I6-5
80	I45	I6-6
81	I46	I6-7
82	I47	I6-8
83	□40	□6-1
84	□41	□6-2
85	□42	□6-3
86	□43	□6-4
87	□44	□6-5
88	□45	□6-6
89	□46	□6-7
90	□47	□6-8
91	□48	□7-1
92	DC GROUND	
93	□49	□7-2
94	□50	□7-3
95	□51	□7-4
96	□52	□7-5
97	□53	□7-6
98	□54	□7-7
99	□55	□7-8
100	□36	□5-5
101	□37	□5-6
102	□38 DET RES	□5-7
103	□39 WDT	□5-8
104	DC GROUND	

C11S PIN ASSIGNMENT

PIN	FUNCTION	
	NAME	PORT
1	□56	□8-1
2	□57	□8-2
3	□58	□8-3
4	□59	□8-4
5	□60	□8-5
6	□61	□8-6
7	□62	□8-7
8	□63	□8-8
9	DC GROUND	
10	I24	I4-1

PIN	FUNCTION	
	NAME	PORT
11	I25	I4-2
12	I26	I4-3
13	I27	I4-4
14	DC GROUND	
15	I48	I7-1
16	I49	I7-2
17	I50	I7-3
18	I51	I7-4
19	I52	I7-5
20	I53	I7-6

PIN	FUNCTION	
	NAME	PORT
21	I54	I7-7
22	I55	I7-8
23	I56	I8-1
24	I57	I8-2
25	I58	I8-3
26	I59	I8-4
27	I60	I8-5
28	I61	I8-6
29	I62	I8-7
30	I63	I8-8

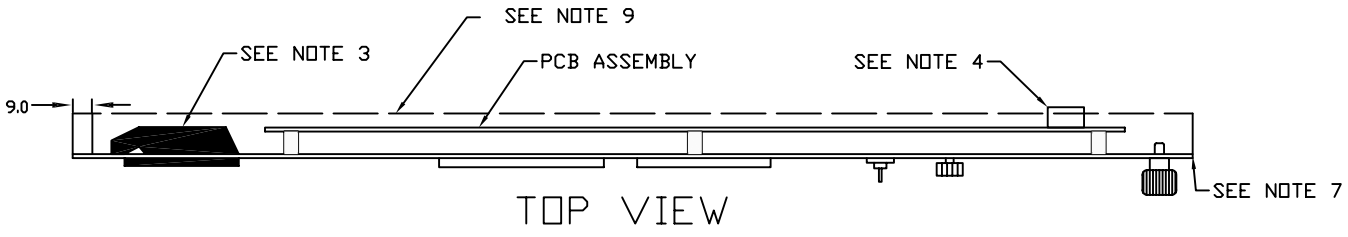
PIN	FUNCTION	
	NAME	PORT
31	DC GROUND	
32	NA	- - -
33	NA	- - -
34	NA	- - -
35	NA	- - -
36	NA	- - -
37	DC GROUND	

TITLE: MODEL 2070-2A
FIELD I/O MODULE
C1 & C11 CONNECTORS

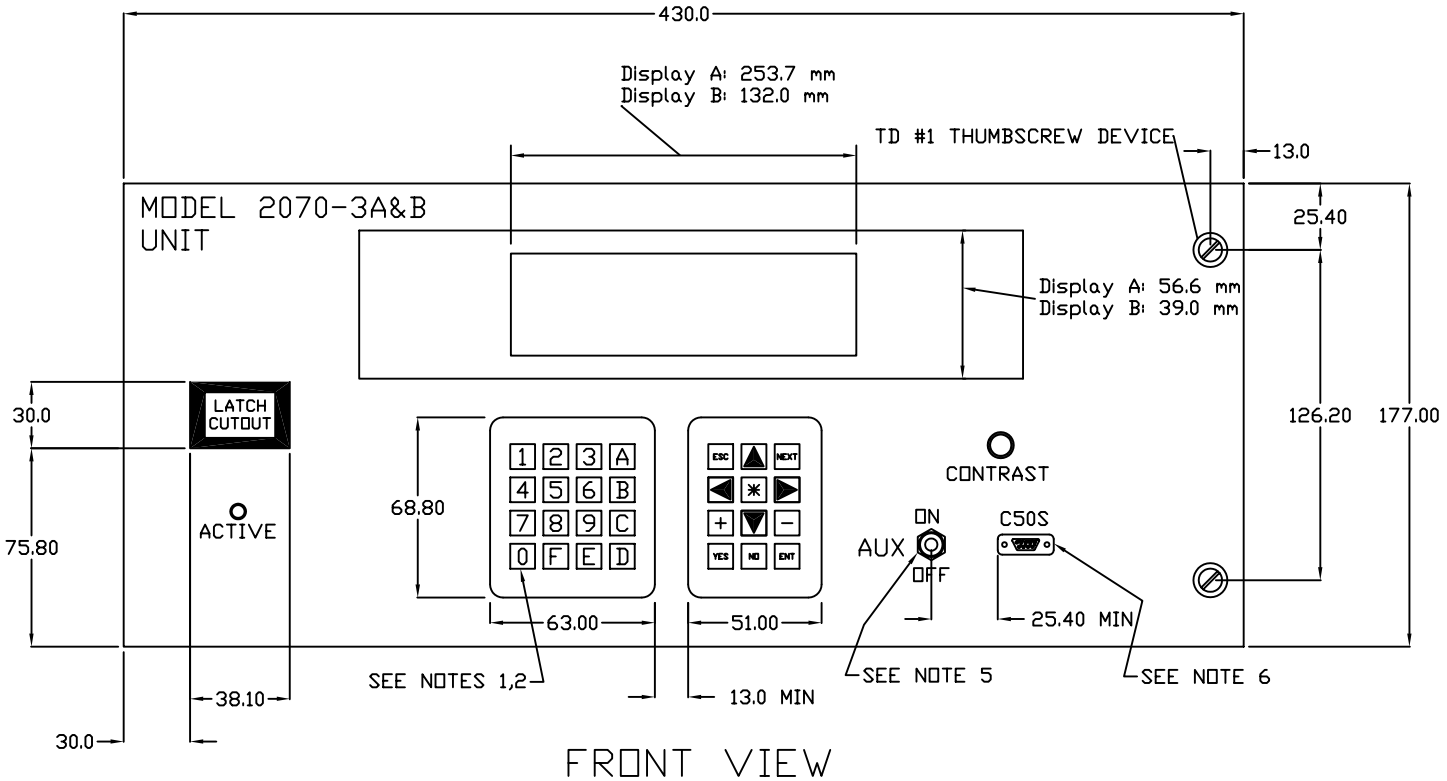
NO SCALE

OCTOBER 27, 2003

9-7-9



TOP VIEW



FRONT VIEW

NOTES (THIS DETAIL)

1. Key size shall be 7.62 X 7.62.
2. Key center to center spacing shall be 12.70 mm.
3. Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
4. 40 contact FP harness pin header connector. It shall be compatible to the FP harness in type and pin assignments. Center of the FP harness header shall be vertically positioned 90 +/- 5 mm as measured from the top of the FPA.
5. Two position CONTROL switch mounted vertically.
6. "C50S" connector shall be a DB-9 socket contact connector.
7. Front panel sheet metal thickness shall be 1.52 ±0.13.
8. All FPA devices shall be located as shown.
9. The FPA shall be provided with a continuous top and bottom 17 mm lip bent 90 degrees to the front plate and shall extend the full length of the FPA.

C50S CONNECTOR PINOUTS	
PIN	C50S FUNCTION
1	C50 ENABLE
2	SP4 RX
3	SP4 TX
4	NA
5	DC GROUND #1
6	NA
7	NA
8	NA
9	NA

C60P CONNECTOR PINOUTS	
PIN	FUNCTION
1	TO POWER B BOX
2	SP6 RX
3	SP6 TX
4	NA
5	DC GROUND #1
6	NA
7	CPU RESET
8	NA
9	CPU LED

TITLE:

MODEL 2070-3A&B FRONT PANEL ASSEMBLY

	NO SCALE	
	OCTOBER 27, 2003	9-7-10

MODEL 2070-3 AUX SWITCH CODES		
SWITCH POSITION	ASCII DATA (TEXT)	ASCII DATA (HEX)
ON	ESC O T	1B 4F 54
OFF	ESC O U	1B 4F 55

MODEL 2070-3 KEY CODES		
KEY	ASCII DATA (TEXT)	ASCII DATA (HEX)
0	0	30
1	1	31
2	2	32
3	3	33
4	4	34
5	5	35
6	6	36
7	7	37
8	8	38
9	9	39
A	A	41
B	B	42
C	C	43
D	D	44
E	E	45
F	F	46
(UP ARROW)	ESC [A	1B 5B 41
(DOWN ARROW)	ESC [B	1B 5B 42
(RIGHT ARROW)	ESC [C	1B 5B 43
(LEFT ARROW)	ESC [D	1B 5B 44
ESC	ESC O S	1B 4F 53
NEXT	ESC O P	1B 4F 50
YES	ESC O Q	1B 4F 51
NO	ESC O R	1B 4F 52
*	*	2A
+	+	2B
-	-	2D
ENTER	CR	OD

TITLE:

MODEL 2070-3
FRONT PANEL ASSEMBLY
KEY CODES

NO SCALE

OCTOBER 27, 2003

9-7-11

CONFIGURATION COMMAND CODES

ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py ; Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Home cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn ; Pn...f	1B 50 P1 5B Pn 3B...Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 5 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 5 l	1B 3B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on -Note 2
ESC [27 l	1B 5B 32 37 6C	Reverse video off -Note 2
ESC [24 h	1B 5B 32 34 68	Underline on -Note 2
ESC [24 l	1B 5B 32 34 6C	Underline off -Note 2
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Clear tab stop Pn = 0,1,2 at cursor = 3 all tab stops
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up

NOTE: 1. Numerical values have one ASCII character per digit without leading zero.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A & B.
Commends shall be available for option 3C (C60).

INQUIRY COMMAND-RESPONSE CODES

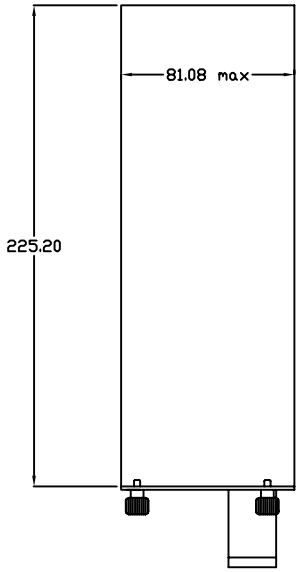
COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Py; Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [B n	1B 5B 42 6E	ESC [P1;P2;.....P6 R	1B 5B P1 3B P2 3B....P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)

TITLE: MODEL 2070-3
FRONT PANEL ASSEMBLY
KEY CODES

NO SCALE

OCTOBER 27, 2003

9-7-12



TOP VIEW

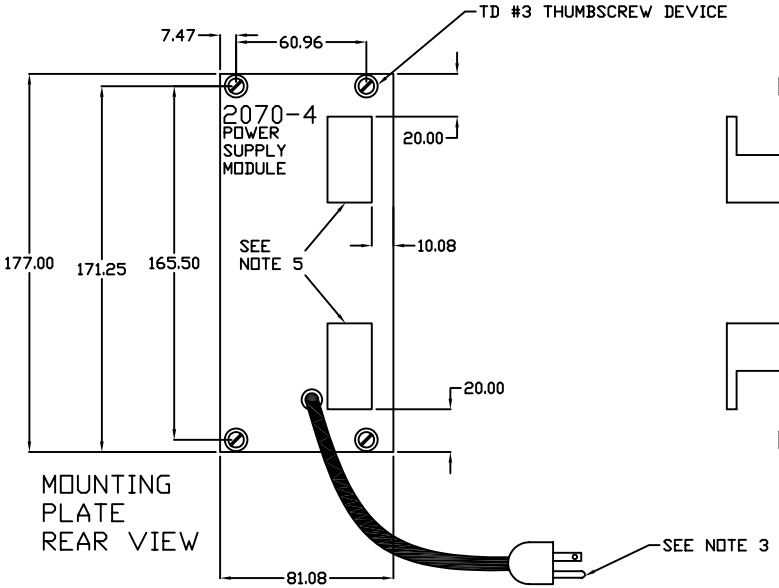
PS1 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	NA

PS2 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC
7	DC GROUND (+12 VDC ONLY)
8	POWER DOWN / AC FAIL
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

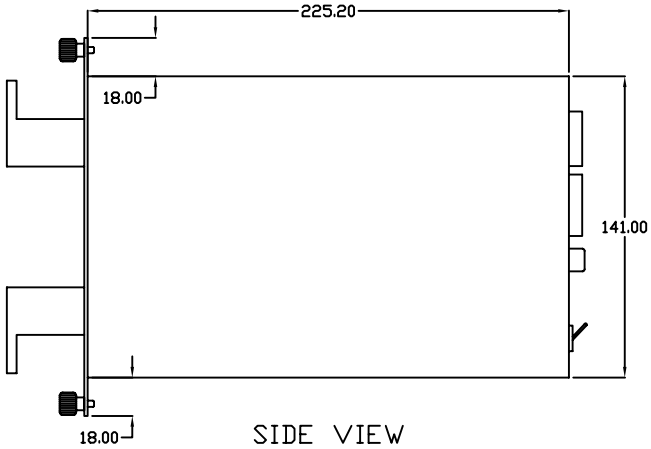
NOTES (THIS DETAIL)

1. Power switch shall be mounted vertically. Power On shall be in the up position.
2. Fuse shall be a replaceable 3AG Slow Blow type resident in a fuse holder. Fuse label shall indicate rating.
3. Three #16 conductor power cable, 1 meter minimum length and permanenlty attached to the Module with strain relief. The end plug connector shall be a three blade NEMA 5-15P grounding plug type.
4. PS1 and PSS2 Receptacle Connectors shall be AMP Mini-Universal Double row MATE-N-LOK CAP Connectors with locking latch devices (OR EQUAL).

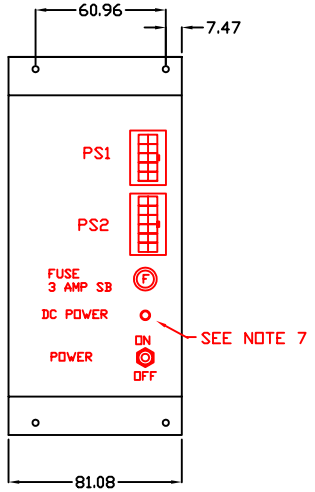
   PS1 connector shall be a 10 position PLUG connector.
   PS2 connector shall be a 12 position PLUG connector.
5. Buckeye Cord-Wrap PP-40055 device with PP-40058 Extension (OR EQUAL).
6. Mounting Plate shall conform to the 4X Wide Module dimensions.
7. A LED indicator shall be provided for each DC power source (+5, +12 ISO, +12 SERIAL, -12 SERIAL).
8. Power Supply will be marked with 2070-4A or 2070-4B



MOUNTING
PLATE
REAR VIEW



SIDE VIEW



FRONT VIEW

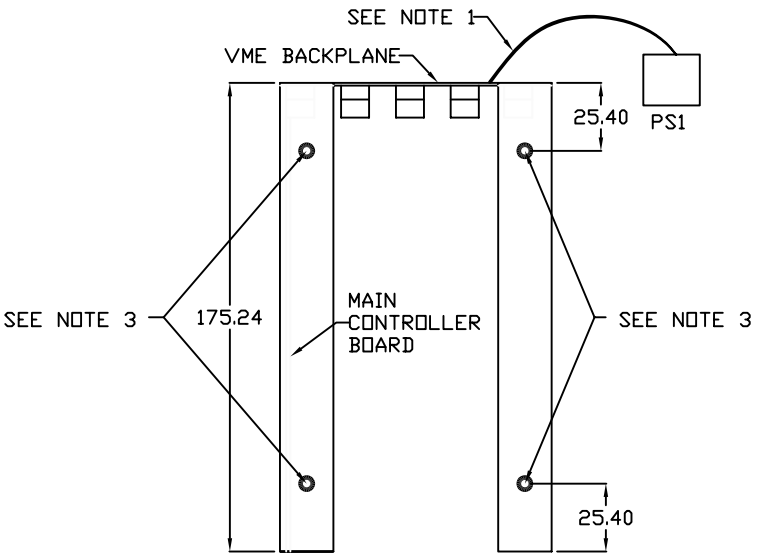
TITLE:

MODEL 2070-4
POWER SUPPLY MODULE

NO SCALE

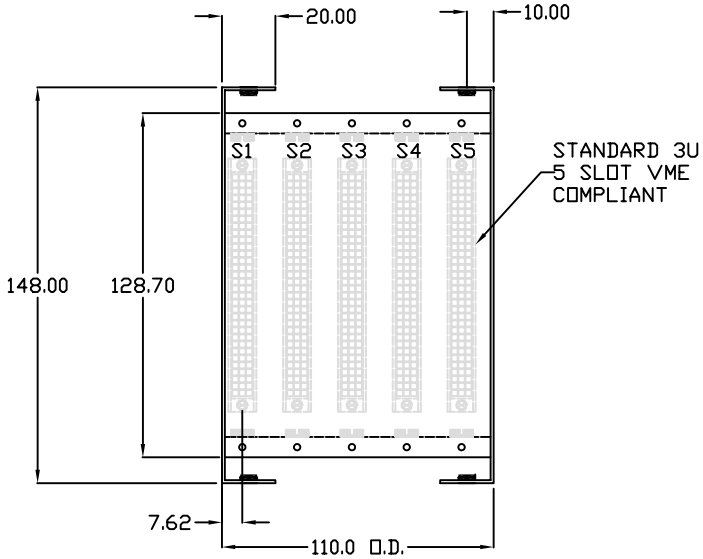
OCTOBER 27, 2003

9-7-13



TOP VIEW

PS1 CONNECTOR PIN ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	NA



FRONT VIEW

NOTES (THIS DETAIL)

1. PS1 Harness interfaces between the Model 2070-4 Power Supply Module and the 2070-5 VME Cage Assembly. The harness shall be permanently attached to the Cage Assembly by solder, FASTON or Power Bugs. The Harness wiring shall be 8 #18 conductors for power and 2 #22 conductors for others.

2. The plate shall cover the open area & attach to the Chassis Backplane mounting surface via screws meeting the Chapter 1 external screw requirements. The screws shall mate with the PEM nuts as specified in the Model 2070 Chassis Top View Detail.

3. G-32 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the 6-32 screws on the top and bottom of the Model 2070 chassis.

TITLE:

MODEL 2070-5
VME CAGE ASSEMBLY

	NO SCALE	
	OCTOBER 27, 2003	9-7-14